REMARKS

Reconsideration of the application is respectfully requested in view of the proposed amendments and the discussion presented below. The proposed amendments are supported by the application as filed and no new matter has been added by the amendment.

The benefit of the Office's policy concerning calculation of the date on which the shortened statutory period will expire is claimed because this paper and the accompanying Rule 131 declaration are filed within two months and two days (a weekend day and a federal holiday) of the mailing date of the final office action.

Claims 1-3 and 19 are proposed to be amended and claims 6-8, 13-17, and 24-32 are proposed to be canceled, as described further below.

The Examiner is respectfully requested to enter the proposed amendments because they would be proper under 37 C.F.R. § 1.116(b)(2) ("[a]n amendment presenting rejected claims in better form for consideration on appeal may be admitted"). In addition, the proposed amendments are believed to be proper under 37 C.F.R. § 1.116(b)(3)("[a]n amendment touching the merits of the application or patent under reexamination may be admitted upon a showing of good and sufficient reasons why the amendment is necessary and was not earlier presented"). The Examiner will recall that that the final office action provided what the Examiner described as "new ground(s) of rejection." The Examiner located and cited new references (principally Hak and Moshrefzadeh, et al.) against the pending claims. The proposed amendments to the claims were suggested by the Examiner or, in the case of claim 2, intended to increase the clarity of the claim.

It is believed that the proposed cancellations and amendments to claims 1-3 and 19 will present the pending claims in better form for appeal.

Furthermore, it is believed that entry of the proposed amendments will place this application in condition for allowance.

The new grounds for rejection of the claims are also addressed in the remarks below.

Claims 1-5, 9-12, and 18-23 will be present in this application if the Examiner accepts the proposed cancellation of claims 6-8, 13-17, and 24-32.

Discussion

1. 'Restriction requirement

The Applicant requests that the Examiner cancel claims 6-8, 13-17, and 24-32 in accordance with the requirement of the Examiner (using form Paragraph 8.24). The Applicant maintains his traversal in order to preserve his right to petition under 37 CFR 1.144.

2. Objection to drawings

The Examiner is believed to have withdrawn his objection to the drawings (see the office action of January 6, 2001). The Applicant traversed the objection in the Amendment and Response filed on April 6, 2006 and the Examiner did not repeat the objection in the office action mailed on July 3, 2006. The Examiner is respectfully requested to confirm that the objection is withdrawn.

3. Objection to claims 1-3 and 19

The objections to claims 20, 22, and 23 are believed to have been withdrawn because the Examiner did not repeat them. The new objection to claims 1-3 and 19 should be withdrawn if the Examiner enters the amendments to these claims proposed in this paper.

The amendments were suggested in the final office action mailed on July 3, 2006. In addition, the language "prior to the step of thinning" is added after "wherein the planar protective layer uniformly covers the defects" in claim 2 for the purpose of clarification.

4. Rejection of claims 1-3, 18, 19, and 21 under 35 USC 102(e) as being anticipated by Hak (US 2004/0018733)

Claims 1-3, 18, 19, and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by US patent application publication 2004/0018733) to Hak ("Hak").

35 U.S.C. § 102(e) states, in pertinent part:

A person shall be entitled to a patent unless –

(e) the invention was described in - (1) an application for patent, published under section 122(b) by another filed in the United States before the invention by the applicant for patent . . . ;

The Section 102(e) rejection of the pending claims over Hak should be withdrawn at least because the Applicant made the claimed invention in the United States of America before the effective filing date of Hak. A declaration of the Applicant pursuant to 37 C.F.R. § 1.131(a) accompanies this paper in order to support the argument for withdrawing the Hak reference.

The filing date of Hak is July 23, 2002. It is respectfully submitted that the accompanying declaration of Peter Brewer, the Applicant, establishes actual reduction to practice of the subject matter of the claimed invention by at least November 8, 2001, and before Hak's effective date. Annex A to this paper correlates the claims against which Hak is cited with the Exhibit describing the invention reduced to practice.

The rejections of claims 1-3, 18, 19, and 21 over the Hak reference therefore should be withdrawn because the Hak reference may not be used as a reference under 35 U.S.C. § 102(e). *See* MPEP § 715.

5. Rejection of claims 4, 5, and 20 under 35 USC 103(a) as being unpatentable over Hak (US 2004/0018733)

Claims 4, 5, and 20 depend from claim 1 directly or indirectly. As noted above, Hak is removed as a reference against claim 1 due to prior invention by the Applicant. The limitations added by claims 4 (thickness range of photoresist layer), 5 (thickness of photoresist layer), and 20 (semiconductor selected from a group consisting of GaSb, InAs, Si, InP, GaAs, InAs, and AlSb) are also disclosed in Applicant's evidence of prior invention.

Hak is not available as a reference against claims 4, 5, and 20 and the Section 103(a) rejection of these claims over Hak should be withdrawn for at least that reason.

6. Rejection of claims 1-3 and 18-20 under 35 USC 103(a) as being unpatentable over Fujisada, et al. (JP 58-18928) in view of Moshrefzadeh, et al. (US 6,077,560)

The Examiner states that Fujisada, et al. disclose the claimed method but do not "expressly teach the protective layer is a planar protective layer that uniformly covers the defect." The Examiner stated that the "claimed shape was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the planar protective layer would yield unexpected result," citing *In re Dailey*, 357 F.2d 669, 149 U.S.P.Q. 47 (C.C.P.A. 1966). Nevertheless, the Examiner cited Moshrefzadeh, et al. as teaching "using the planar protective layer (40, fig. 2b) to uniformly cover defects

(protrusion unwanted portions of material 44, figs 2b-2d) in a process of removing defects."

Numbered paragraph [0018] of page 5 of the specification of the instant application, states that "[i]t is preferable that the height of the photoresist layer exceeds the height of the defects to ensure that the resulting surface is planar, in order to enable defects to be successfully revealed during a subsequent thinning process." The claimed "planar" shape is not a mere design choice as was the specific shape of the collapsible infant's bottle in the *In re Dailey* case.

Furthermore, Fujisada, et al. teach away from using a planar surface. Fujisada, et al. teach applying a resist 3 by dropping it to the surface of an epitaxial wafer 1 that is rotating at high speed. The film of resist covering the protrusions 2 thereby becomes "far thinner" than other portions of the resist 2 covering the rest of the epitaxial wafer 1. As seen in the drawings, the film-coated protrusions 2 rise above the resist 3 covering the rest of the surface of the epitaxial wafer 1. The thinner film is selectively removed from the protrusions 2 so that the protrusions 2 can be removed by being etched, with the remaining resist 3 acting as a mask. The protrusions 2 have a thinner film of resist 3 precisely because the resist 3 does not have a planar surface.

Moshrefzadeh, et al. teach one embodiment of a process for continuous and maskless patterning of structured substrates in which a patterned surface having a plurality of protrusions is covered by flooding it with a filler material thick enough to cover the protrusions and planarizing the filler coating using a blade, a release liner such as a thin, flexible stainless steel sheet, a coating roll, and the like. Col. 4, line 49 to col. 5, line 11. The filler coating may be a "photosensitive resist material as may be employed in conventional lithography." Col. 5, lines 41-42. The filler material is thereafter partially removed in a uniform fashion to expose only those portions of the protrusions that are to

be modified. Col. 5, lines 29-44. After modification by, for example, etching or deposition, the remaining filler material may be removed, resulting in a structured substrate selectively modified or patterned at its protrusions. Col. 7, lines 6-26. The Examiner is incorrect to say that Moshrefzadeh, et al. teaches a "process of removing defects" because Moshrefzadeh, et al. does not teach or suggest removal of the protrusions.

A *prima facie* case of obviousness with respect to claim 1 is not established because the Examiner has not correctly articulated a basis for concluding that it would have been obvious to make the claimed invention using the combination of the Fujisada, et al. and Moshrefzadeh, et al. references. The Examiner does not correctly identify a suggestion or motivation for combining features of these references because he misinterprets Moshrefzadeh, et al. as being directed to a process for the removal of defects. He also fails to note that Fujisada, et al. teaches against using a planar surface. Without substantial evidence of a motivation, suggestion or teaching to combine the cited references without knowledge of the invention, one can only conclude that the Examiner has employed the claim as his sole guide for combining the references – in other words, hindsight. This is clear error. *See* M.P.E.P. at section 2143.01, *accord* In re Rouffet, 47 USPQ2d 1451, 1457-58 (Fed. Cir. 1998)("[t]o prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness").

Claims 2, 3, and 18-20 depend directly or indirectly from claim 1. As explained above, Fujisada, et al. and Moshrefzadeh, et al. do not teach or suggest the method of claim 1. For at least this reason claims 2, 3, and 18-20 are allowable over these references.

The suggested combinations and modifications therefore do not teach or suggest the limitations of claims 1-3 and 18-20 and a *prima facie* case of obviousness is not established. This rejection should be withdrawn.

7. Rejection of claims 4, 5, and 9-12 under 35 USC 103(a) as being unpatentable over Fujisada et al. (JP 58-18928) in view of Moshrefzadeh, et al. (US 6,077,560) as applied to claim 3 and further in view of Kudo, et al. (JP 63-216346) or Chiu, et al. (US 6,955,177)

The Examiner states that Fujisada, et al. in view of Moshrefzadeh, et al. as applied to claim 3 "substantially discloses" the claimed method with the exception of "how to thin the planar protective layer of the photoresist layer" (claims 9, 11, and 12). The limitations added by these claims are stated to be "known techniques to etch/remove photoresist material," citing Chiu, et al and Kudo, et al. as "evidences that shows using ICP oxygen process, RIE or ERC for removing photoresist material" and "therefore, at the time of the invention, it would have been obvious for those skilled in the art, in view of Chiu, et al. or Kudo, et al., to use the ICP oxygen process, RIE or ERC as known technique in the thinning step process of Fujisada, et al. in view of Moshrefzadeh, et al. to reveal portions of the defects for removing said defects to provide a better semiconductor device."

The Examiner also states that Fujisada, et al. in view of Moshrefzadeh, et al. as applied to claim 3 "substantially discloses" the claimed method with the exception of the "claimed range thickness of the photoresist layer and the etch rate of the thinning process" (claims 4, 5, and 10). These limitations are "considered to involve routine optimization while [sic] has been held to be within the level of ordinary skill in the art" and these claims are "prima facie obvious without showing that the claimed ranges achieve unexpected results."

Claims 4, 5, and 9-12 depend directly or indirectly from claim 1. As explained above, Fujisada, et al. in view of Moshrefzadeh, et al. do not teach or suggest the claimed method of claim 1. The Examiner has not asserted that Chiu, et al and Kudo, et al. teach or

suggest the limitations of the method of claim 1. The suggested combinations therefore cannot teach or suggest the limitations of claims 4, 5, and 9-12 and a *prima facie* case of obviousness is not established.

It should be noted that the Chiu, et al. reference is not usable against this application. Chiu, et al. was filed on December 7, 2001 and issued on October 18, 2005. It is available against the present application only under 35 U.S.C. § 102(e). The accompanying declaration of Peter Brewer shows that the invention was made at least by November 8, 2001.

Furthermore, the *prima facie* case of obviousness is not established because the Examiner has not identified the suggestion or motivation for combining the features of the Fujisada, et al., Moshrefzadeh, et al., Chiu, et al and Kudo, et al. references, or for the routine optimization, other than the blueprints provided by claims 4, 5, and 9-12. As observed above, this is error and a further reason why the *prima facie* case of obviousness has not been established.

For at least these reasons a *prima facie* case of obviousness has not been established and this rejection should be withdrawn.

8. Rejection of claims 21-23 under 35 USC 103(a) as being unpatentable over Fujisada et al. (JP 58-18928) in view of Moshrefzadeh, et al. (US 6,077,560) as applied to claim 1 above, and further in view of Takehiko, et al (JP 06041770) or Starzynski (US 2005/0065050)

The Examiner states that Fujisada, et al. in view of Moshrefzadeh, et al. "substantially discloses the claimed method including removing the defects from the semiconductor surface by etching," but do not "expressly teach using a wet chemical etchant (claim 21)" or chemical etchants selected from the groups recited by claims 22 or

23. Takehiko, et al. and Starzynski, et al. are cited as teaching "using the wet chemical etchant to clean/remove defects to [sic] the semiconductor surface." "Selection of a known material based on its suitability for its intended use" was stated to be prima facie obvious based on the authorities of *Sinclair & Carroll Co. v. Interchenical Corp.*, 325 U.S. 327, 65 U.S.P.Q. 297 (1945) and *In re Leshin*, 227 F.2d 197, 125 U.S.P.Q. 416 (C.C.P.A. 1960).

Claims 21-23 depend directly or indirectly from claim 1. As explained above, Fujisada, et al. in view of Moshrefzadeh, et al. do not teach or suggest the claimed method of claim 1. The Examiner has not asserted that Takehiko, et al. and/or Starzynski, et al., or the "selection of a known material based on its suitability for its intended use" teach or suggest the limitations of the method of claim 1. The suggested combinations therefore cannot teach or suggest the limitations of claims 21-23 and a *prima facie* case of obviousness is not established.

Furthermore, the *prima facie* case of obviousness is not established because the Examiner has not identified the suggestion or motivation for combining the features of the Fujisada, et al., Moshrefzadeh, et al., Takehiko, et al. and/or Starzynski, et al. references, or for the "selection of a known material based on its suitability for its intended use," other than the blueprints provided by claims 21-23. As observed above, this is error and a further reason why the *prima facie* case of obviousness has not been established.

Finally, it should be noted that the Starzynski, et al. reference is not usable against this application. Starzynski, et al. was filed on April 19, 2004, published on March 24, 2005, and asserts priority from a provisional application filed on September 23, 2003. It is available against the present application only under 35 U.S.C. § 102(e). Even if the earlier date of the provisional application is available, Starzynski, et al.'s effective date would still be well after the date the invention of the instant application was made. The

accompanying declaration of Peter Brewer shows that the invention was made by at least November 8, 2001.

Conclusion

In view of the above, the Applicant submits that the application is now in condition for allowance and respectfully urges the Examiner to pass this case to issue. The Examiner is respectfully invited to telephone the undersigned attorney as needed in order to advance the examination of this application.

* * *

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

REPLY UNDER 37 C.F.R. § 1.116 – EXPEDITED PROCEDURE –
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I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office (USPTO) on the date shown below. Specifically, this correspondence is being telefaxed to Examiner Thanhha S. Pham at the USPTO at 571-273-8300 on September 5, 2006. (Date of Transmission) Aileen M. Shrestha (Name of Person Transmitting) Aileen Shrestha (Signature) September 5, 2006 (Date)	Respectfully submitted, R. Dabney Eastham Attorney for Applicants Reg. No. 31,247 LADAS & PARRY LLP 5670 Wilshire Boulevard, Suite 2100 Los Angeles, California 90036 (323) 934-2300 voice (323) 934-0202 facsimile reastham@ladas.com

Annex I: Claims rejected over Hak correlated to Exhibit A of Rule 131 Declaration of Peter D. Brewer

Claims (including proposed amendments)	**Exhibit A (report dated November 8, 2001), page 2**
1. A method for removing defects from a semiconductor surface, comprising:	"a self-masking process for removing growth defects from the surface of the MBE grown Sb-based epilayers"
coating the semiconductor surface and the defects with a planar protective layer;	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
thinning the planar protective layer to selectively reveal portions of the defects;	"dry-etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface)"
removing the defects; and	"wet chemical etching of the exposed defect structures"
removing the planar protective layer.	"stripping of the remaining photoresist layer"
2. The method of claim 1 wherein the planar protective layer uniformly covers the defects.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
3. The method of claim 1 wherein the planar protective layer is a photoresist layer.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
4. The method of claim 3 wherein the photoresist layer has a thickness from about 5	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"

Claims (including proposed amendments)	Exhibit A (report dated November 8, 2001), page 2
to about 10 microns.	
5. The method of claim 4 wherein the photoresist layer has a thickness of about 8 microns.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
18. The method of claim 1, wherein removing of the defects is performed by etching.	"wet chemical etching of the exposed defect structures"
19. The method of claim 1, wherein thinning the planar protective layer is performed by a process which is identical to a process for removing the planar protective layer.	"stripping of the remaining photoresist layer"
20. The method of claim I, wherein the semiconductor surface comprises a semiconductor selected from a group consisting of GaSb, InAs, Si, InP; GaAs, InAs, and AlSb.	"a self-masking process for removing growth defects from the surface of the MBE grown Sb-based epilayers"
21. The method of claim 1, wherein the defects are removed using a wet chemical etchant.	"wet chemical etching of the exposed defect structures"